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DELIVERABLE REPORT

WP13 - JA3 Nano-engineering and pattern transfer methods

D13.4
Library of processes based on advanced nano-engineering for TA

This initiative has received funding from the EU's H2020 framework program
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D – 13.4	Library of processes based on advanced nano-engineering for TA

DELIVERABLE DESCRIPTION

In the current document we report on a selection of new processes developed within the NFFA (NEP) project related to advanced nanoengineering for transnational access (TA). They form a new library of process steps enabling new or improved capabilities for some specific nanopatterning. They are complementary and generally compatible with state-of-the-art microelectronics industry. Besides developing the individual core technology, we paid particular attention to novel groupings in a mix-and-match approach to study possible combinations of processes to maximize enabling capabilities for nanosystems manufacturing.

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NATURE

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☐ P - Prototype

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☐ CO - Confidential, only for members of the consortium

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SUMMARY

In the following we report on a selection of new nanofabrication processes developed within the NFFA (NEP) project related to advanced nanoengineering for transnational access (TA). They form a new library of process steps enabling new or improved capabilities for some specific nanopatterning with a focus on lithography and patternn transfer. They are complementary and compatible with state-of-the-art microelectronics industry processes. Besides developing the individual core technology, we paid particular attention to novel groupings in a mix-and-match approach to study possible combinations of processes to maximize enabling capabilities for nanosystems manufacturing. They include:

Nanofabrication process	**Acronym**
Thermal scanning probe lithography	t-SPL
Direct laser writing (direct write litho)	DWL
Nano imprint lithography	NIL
Directed self assembly	DSA
Atomic layer etching	ALE
Dry etching	DE

The following table provide an overview of the considered methods and combinations thereof:

Techniques	**Partner**	**Readiness (A:high to D:low)**	**Comments**
t-SPL + dry etching	EPFL	B	service from cleanroom required to be established
t-SPL + DWL	EPFL	B	service from cleanroom required to be established
t-SPL + grayscale NIL	EPFL	C	additional development and service from cleanroom required to be established
T-SPL + DSA	EPFL & CNM	C	additional development and service from cleanroom required to be established
Talbot Lithography	Lund	A	well established
Mix-match EBL-UV SiNW	CNM	A	well established
Silica resist He-FIB	C2N	C	additional development steps required

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ALE	Lund	D	process under development
Selective area growth of III-V nanowire	C2N	A	well established

In the following pages, each of the method will be presented with process details, exemplary results and further information for the users to efficiently adopt the new techniques for their own purposes. Contact details of the expert groups are also listed, so that further collaboration or services can be arranged bilaterally.

Grayscale thermal scanning probe lithography (t-SPL) + dry etching

Grayscale nanopatterning in thin film dielectrics

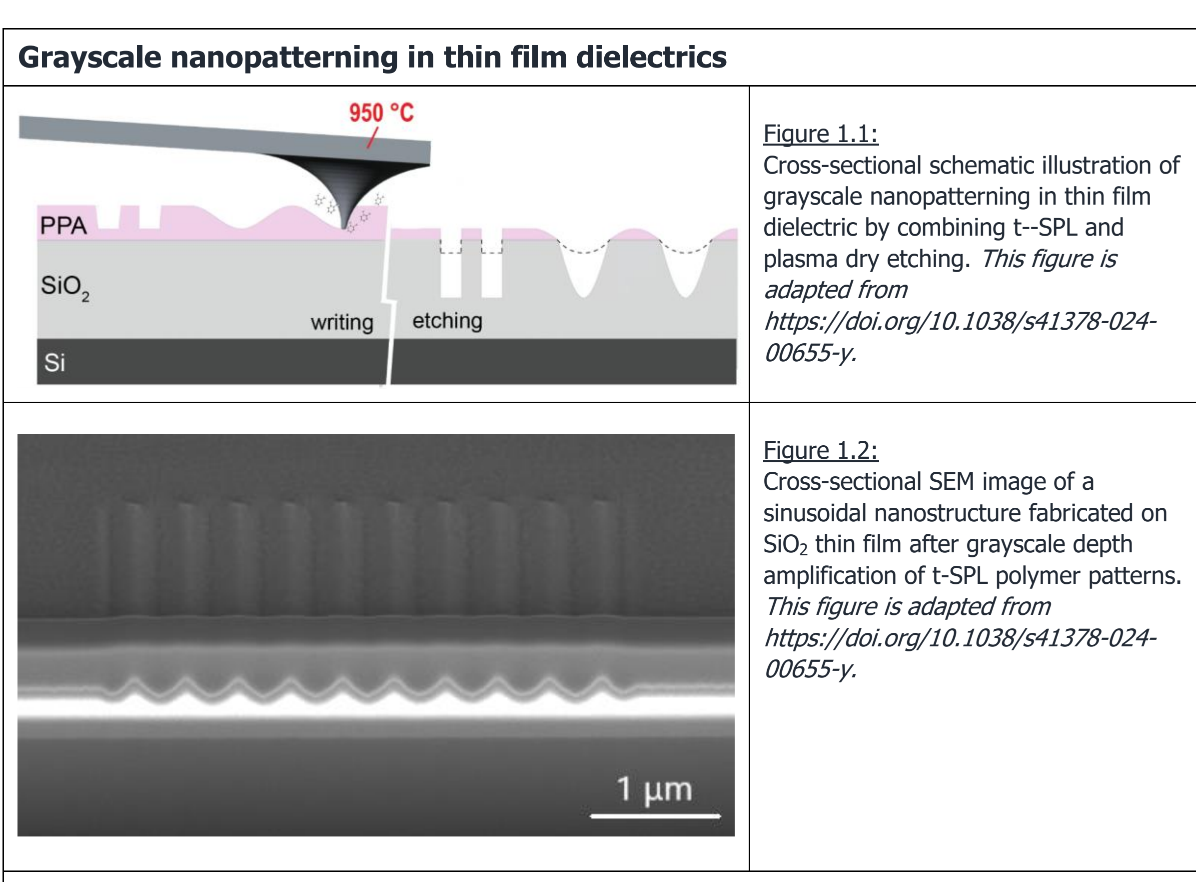

Figure 1.1:
Cross-sectional schematic illustration of grayscale nanopatterning in thin film dielectric by combining t--SPL and plasma dry etching. *This figure is adapted from https://doi.org/10.1038/s41378-024-00655-y.*

Figure 1.2:
Cross-sectional SEM image of a sinusoidal nanostructure fabricated on SiO_2 thin film after grayscale depth amplification of t-SPL polymer patterns. *This figure is adapted from https://doi.org/10.1038/s41378-024-00655-y.*

Process: This process combines single-digit nanometer-precision nanopatterning in the x, y, and z axes using t-SPL followed by plasma dry etching. Etch selectivity between thermal resist polyphthalaldehyde (PPA) and SiO_2, as well as control of substrate temperature during plasma etching with a He-based cooling cycle, allow for pattern depth amplification of up to 10-fold. This technique amplifies grayscale polymer nanopatterns, such as rectangular and sinusoidal nanopatterns, when transferred in thin-film dielectrics, achieving a significant increase in depth without introducing additional surface roughness.

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Purpose: t-SPL achieves a single-digit nanometer lateral resolution and a vertical resolution down to below 1 nm, but its maximum depth in polymers is limited, typically to 100 nm. The combination of nanowriting in thermal resist and plasma dry etching overcomes the limitation in grayscale nanopatterning depth.

Major challenges in process:

- Repeatable t-SPL patterning depending on actual heated nanotip size
- Etch selectivity control of plasma with parameters of gas composition and its flow rate, pressure, RF bias power, and substrate temperature

Applications: Grayscale nanopatterns are used in nanofluidics for bioparticle analysis, optical gratings for more precise control over a diffracted wavefront compared to binary-shaped conventional gratings, and strain engineering of 2D materials for nanoelectronic applications.

Advantages:

- Enhanced lateral and vertical resolutions of t-SPL compared to grayscale e-beam lithography and interference lithography
- Smooth pattern transfer and grayscale nanopattern amplification with CHF_3/SF_6 plasma

Limitations:

- Patterning on conductive substrates due to required electrostatic actuation
- Limited throughput of t-SPL with piezo movement range of up to 60 µm
- Tip abrasion and nanotip dependent pattern resolution
- Limited to thermally sensitive materials as heat is the main stimulus of t-SPL

References :

[1] Howell, Samuel Tobias, et al. "Thermal scanning probe lithography—a review." *Microsystems & nanoengineering* 6.1 (2020): 21.
[2] Erbas, Berke, et al. "Combining thermal scanning probe lithography and dry etching for grayscale nanopattern amplification." *Microsystems & Nanoengineering* 10.1 (2024): 28.
[3] Kirchner, R., Guzenko, V. A., & Schift, H. (2019). Single-digit 6-nm multilevel patterns by electron beam grayscale lithography. *Advanced Optical Technologies*, *8*(3-4), 175-180.
[4] Fallica, Roberto, et al. "High-resolution grayscale patterning using extreme ultraviolet interference lithography." *Microelectronic Engineering* 177 (2017): 1-5.
[5] Skaug, Michael J., et al. "Nanofluidic rocking Brownian motors." *Science* 359.6383 (2018): 1505-1508.
[6] Lassaline, Nolan, et al. "Optical fourier surfaces." *Nature* 582.7813 (2020): 506-510.

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Mix-and-match lithography: t-SPL and DWL lithography combining thermal scanning probe lithography (t-SPL) with DWL lithography.

t-SPL / DWL seamless process

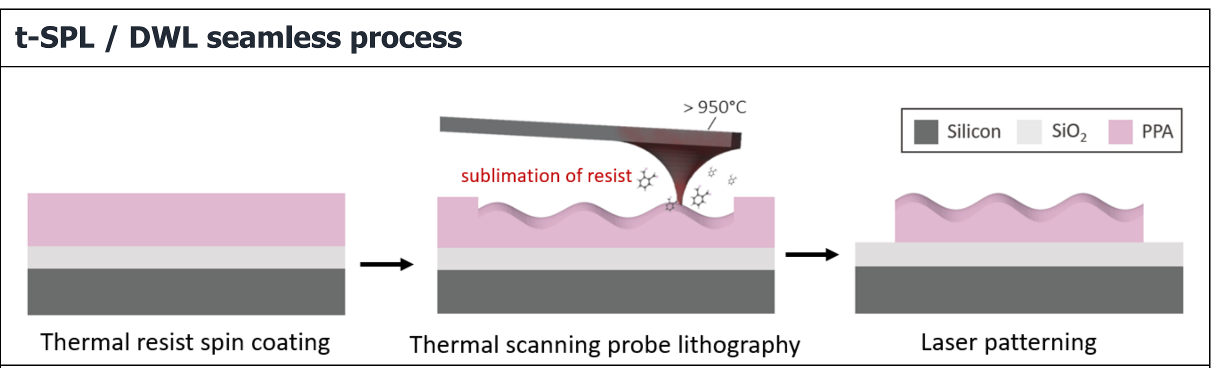

Figure 2.1:
Cross-sectional schematic illustration of mix-and-match process combining thermal scanning probe (t-SPL) and direct-write laser lithography (DWL lithography) seamlessly

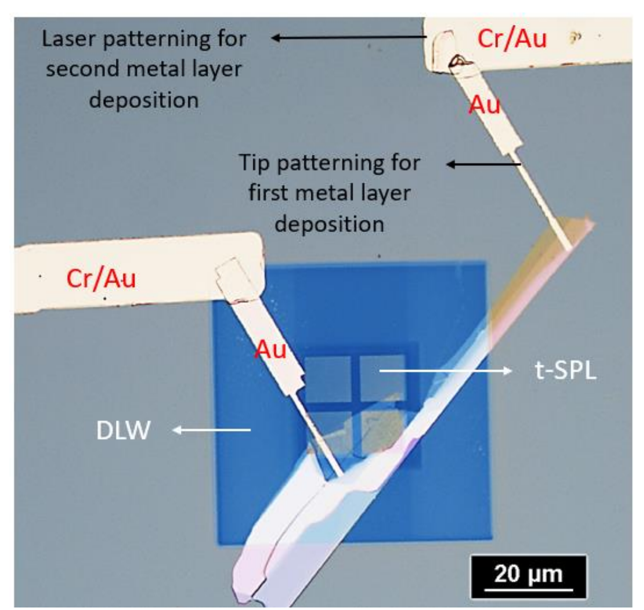

Figure 2.2:
Combination of t-SPL and DWL lithography for fabrication of multi-scale grayscale micro- and nano-structures as well as contact electrodes pads of 2D materials-based FET.

Process: This process uses a hybrid approach to create electrode contacts using a seamless combination of thermal scanning probe lithography (t-SPL) and direct-write laser lithography (DWL lithography). This strategy involves employing t-SPL for patterns located precisely on a semiconductor channel and DWL lithography for larger features positioned farther away from the 2D material. The patterning of 2D materials is achieved using t-SPL for smaller (<100 nm) and DWL lithography for larger (> 1 µm) features, respectively. Tip patterning speeds are approximately 6000 μm^2/min, whereas DWL lithography offers about 20 times faster patterning speeds. Combining t-SPL and DWL lithography enables markerless overlay with sub-1 µm accuracy, reducing lithography time. By combining tip patterning with laser sublimation, it is possible to fabricate corrugated nanostructures that strain 2D semiconductor materials transferred onto them. Contacts were patterned using a mix-and-match approach, with t-SPL used for small features atop the 2D materials and DWL lithography for larger features away from the materials.

Purpose: t-SPL offers advantages over charge-based lithography for nano-processing on sensitive materials such as 2D materials, quantum dots, and nanotubes. Given the rapid progress in the field of 2D materials,

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particularly 2D semiconductors, there is a growing need for charge-free and damage-free manufacturing processes of these ultra-thin material.

Major challenges in process:

- Alignment of tip and laser patterns
- Tip patterning on non-flat corrugated surfaces

Applications: Grayscale and binary patterns used for micro-nano- fluidics, optics and electronics, strain engineering of 2D materials on pre-patterned substrates, metal-2D semiconductor contact engineering, combined binary and grayscale patterning.

Advantages:

- Charge-free patterning with heat-based polymer sublimation
- Low substrate temperature due to localized depolymerization of PPA resist during endothermic reaction
- Increased throughput with combined t-SPL and DWL lithography
- Surface topography imaging and markerless overlay

Limitations:

- Patterning on conductive substrates
- Limited throughput of tip patterning and its size dependent resolution
- Very limited instantaneous depth correction on grayscale topographies through closed-loop feedback, unlike accurate depth correction on flat surfaces
- Increased tip abrasion in contact with non-flat surfaces

References :

[1] Conde-Rubio, Ana, et al. "Edge-contact MoS2 transistors fabricated using thermal scanning probe lithography." *ACS applied materials & interfaces* 14.37 (2022): 42328-42336.
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[3] Rawlings, Colin, et al. "Accurate location and manipulation of nanoscaled objects buried under spin-coated films." *ACS nano* 9.6 (2015): 6188-6195.
[4] Rawlings, Colin, et al. "Fast turnaround fabrication of silicon point-contact quantum-dot transistors using combined thermal scanning probe lithography and laser writing." *Nanotechnology* 29.50 (2018): 505302.

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Grayscale nanoimprint stamps

Grayscale nanopatterns replication

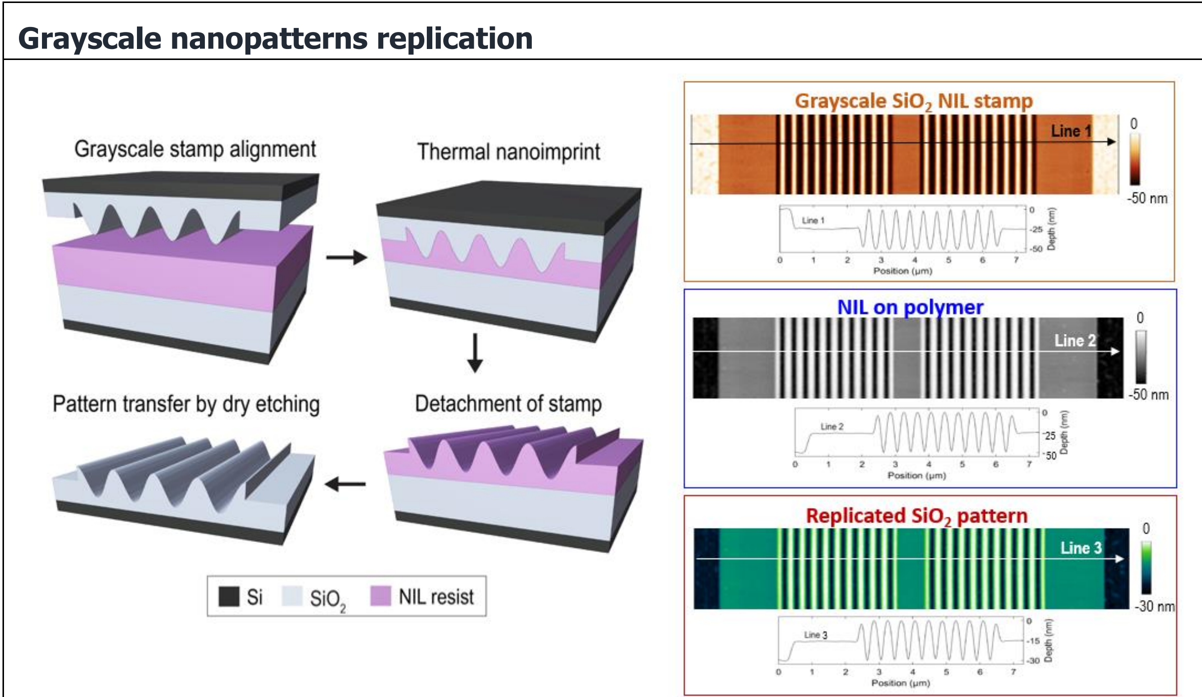

Figure 3.1:
Fabrication process flow of thermal nanoimprint lithography using grayscale stamps and AFM images of stamps, replicated nanopatterns on thermoplastic resist and after pattern transfer onto SiO_2. *This figure is adapted from https://doi.org/10.1038/s41378-024-00655-y.*

Process: This process combines thermal scanning probe lithography (t-SPL) with dry etching to fabricate grayscale nanoimprint lithography (NIL) stamps, addressing the limited throughput of t-SPL. This grayscale stamp, which is coated with anti-stiction layer, is then employed to replicate nanopatterns onto a thermoplastic NIL resist and subsequently transferred onto thin dielectric films on wafers.

Purpose: NIL provides a cost-effective method for replicating high-resolution grayscale nanostructures on large surfaces through a step-and-repeat process. This integrated approach of t-SPL, NIL, and dry etching techniques holds promise for the upscaled manufacturing of grayscale patterns with enhanced functionality and efficiency.

Major challenges in process:

- Incomplete filling of polymer
- Alignment
- Grayscale pattern deformation during multiple plasma etch transfers

Applications: Grayscale patterns used for micro-nano- fluidics, optics and electronics, strain engineering of 2D materials on pre-patterned substrates

Advantages:

- Repeatable replication of high-resolution nanostructures
- Cost-efficient and energy-efficient fabrication technique

Limitations:

- Required step-and-repeat process with precise alignment for wafer-scale fabrication
- Relatively high temperature (~200 °C) and long process (~30 mins)

References :

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[1] Erbas, Berke, et al. "Combining thermal scanning probe lithography and dry etching for grayscale nanopattern amplification." *Microsystems & Nanoengineering* 10.1 (2024): 28.
[2] Schift, Helmut. "Nanoimprint lithography: 2D or not 2D? A review." *Applied Physics A* 121 (2015): 415-435.

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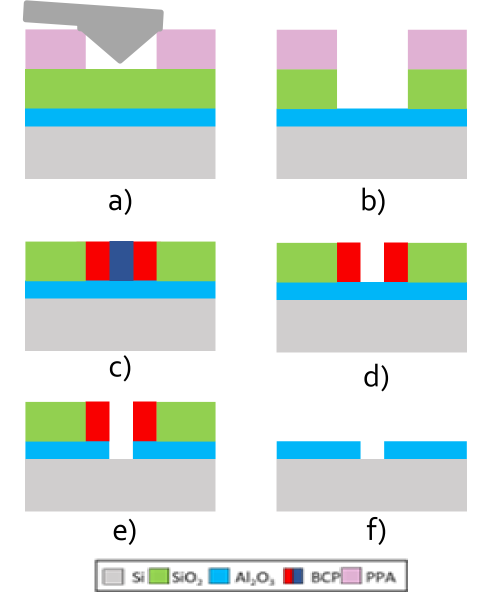
Hole shrink by thermal-SPL and DSA

Nanometer scale apertures created by the combination of t-SPL and DSA



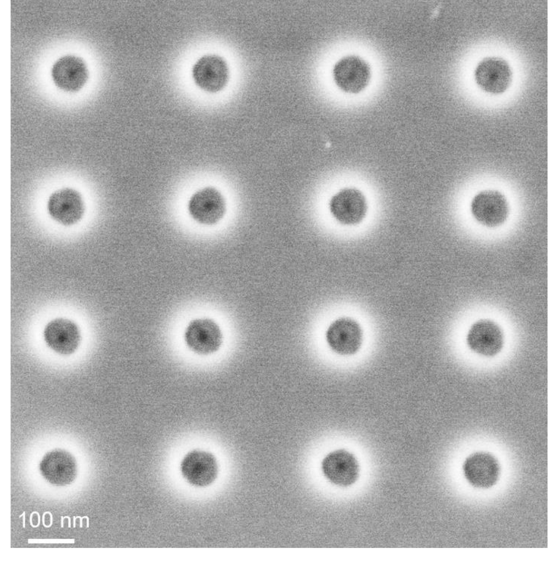


Figure 4.1: Cross-sectional schematic illustration of mix-and-match process combining thermal scanning probe (t-SPL) and directed self-assembly of block copolymers (BCP) for contact hole shrink. a) t-SPL patterning by PPA sublimation in contact with hot tip. b) Pattern transfer to SiO_2 hardmask by reactive ion etching (RIE). c) Directed self-assembly of BCP. d) PMMA block removal by wet etching. e) Pattern transfer to Al_2O_3 layer by RIE. f) Remaining polymer and SiO_2 hard mask removal.

Figure 4.2: Top view SEM image of pattern hole shrink on circular t-SPL defined patterns. The image is taken after step (e) in Figure 4.1. As it can be observed, the diameter of the hole is reduced from 50 nm to 15 nm.

Process: combination of thermal scanning probe lithography (t-SPL) with directed self-assembly (DSA) of block copolymers (BCPs) as a suitable lithography process to fabricate high-resolution nanometer scale holes.

The combined t-SPL+DSA process is depicted in Figure 4.1. First, two hard mask layers are deposited over the sample by atomic layer deposition (ALD): a top SiO_2 layer, that will serve as guiding pattern, and a bottom Al_2O_3 layer as an etch stopper for SiO_2. Then, a Polyphthalaldehyde (PPA) resist layer is spin-coated and a circular pattern is lithographed by t-SPL. After transferring the pattern into the SiO_2 layer, using the pattern transfer process also developed in this project [1], the defined holes are used as guiding patterns for the DSA of cylindrical PS-b-PMMA BCPs. Then, the minority block, the PMMA cylinder, is selectively removed by wet etching, resulting in a pattern shrink of around 80% in diameter [2]. Finally, the patterned holes are transferred into the Al_2O_3 hard mask via dry etching and the PS and SiO_2 layers are removed. Pattern holes shrinkage by DSA is presented in Figure 4.2 after pattern transfer into the Al_2O_3 hard mask and BCP removal.

Purpose: The main advantage of using t-SPL lies in its high-placement accuracy related to its dual patterning and imaging capabilities. Combining t-SPL with DSA of BCP allows to improve resolution, even beyond what is achievable with top-down lithography, with an unprecedented overlay alignment [3].

Major challenges in process:

- Shape and dimensional control of the holes defined by t-SPL
- T-SPL tip endurance
- Vertical profile of the guiding pattern holes

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- Optimal conditions for the block co-polymer deposition

Applications:

From its inception, the semiconductor industry has strived to improve integrated circuit performance by constantly decreasing device size. In recent years, obtaining precisely placed ultra-small nanoholes has become of interest for applications such as the fabrication of semiconductor qubit devices, where a precise contact of a very dense array of nanoscale gate electrodes is required. To achieve this, lithography methods like deep ultraviolet (DUV) optical lithography and electron beam lithography (EBL) are commonly employed. Now, a combined t-SPL and DSA lithography process is presented for high-alignment accuracy and high-resolution hole patterning. Initial results demonstrate promising outcomes for both pattern hole shrinkage and pattern hole multiplication processes with a process window study being currently underway. In the future, the integration of hole shrink and hole multiplication techniques into semiconductor quantum device fabrication processes will be investigated.

Advantages:

- It allows for high resolution patterning on insulating surfaces (in comparison with EBL)
- Much simpler instrumentation, lower cost in comparison with DUV or EUV lithography
- Potential outstanding overlay alignment

Limitations:

- Limited throughput of tip patterning
- Limited area of tip patterning
- Tip abrasion
- Resolution limited to PS-b-PMMM molecule size. Higher resolution possible by using high-Chi block copolymers
- Low etching selectivity between PS and Al_2O_3

References :

[1] Erbas, Berke, et al. "Combining thermal scanning probe lithography and dry etching for grayscale nanopattern amplification." *Microsystems & Nanoengineering* 10.1 (2024) 28.

[2] A. Gharbi et al., "Contact holes patterning by directed self-assembly of block copolymers: process window study", J. Micro/Nanolith. MEMS MOEMS, 14 (2015) 023508,

[3] S. Gottlieb, et al., "Thermal scanning probe lithography for the directed self-assembly of block copolymers" Nanotechnology 28 (2017) 175301

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SiNW devices by Mix-match Electron Beam and UV lithography

Wafer scale fabrication of silicon nanowire devices

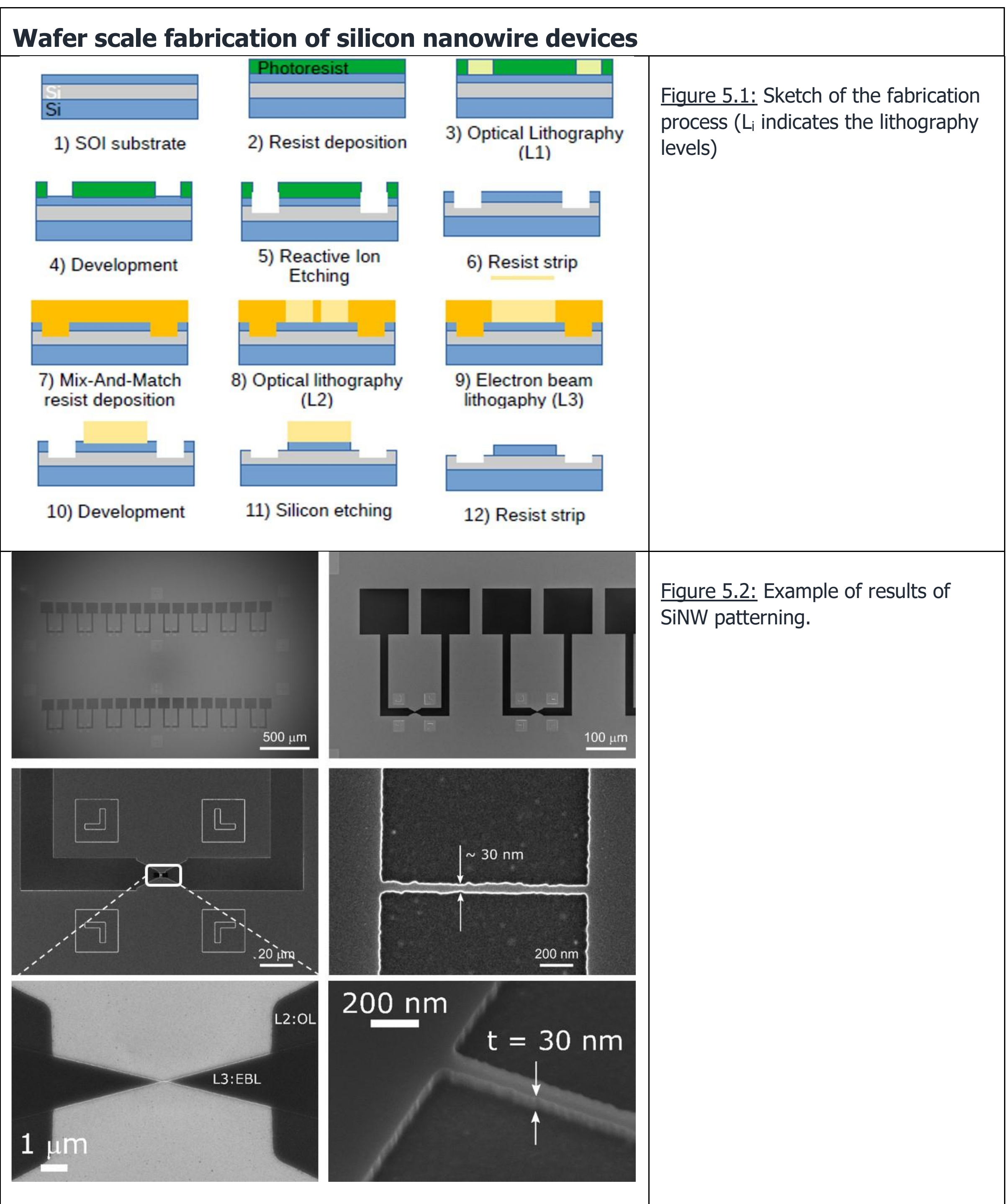

Figure 5.1: Sketch of the fabrication process (L_i indicates the lithography levels)

Figure 5.2: Example of results of SiNW patterning.

Process: We are developing a wafer-scale fabrication process of silicon nanowire (SiNW) devices. The main feature of the process is the use of a resist which is sensitive to optical lithography and electron beam lithography. This reduces the number of process steps and facilitates integration. The fabrication process (see Figure 5.1) consists of 3 levels of lithography (which will be indicated in the following by L_i). We start from a SOI wafer and we define the alignment marks by means of optical lithography (L_1) and reactive ion etching. Then, we deposit the resist AR-N 7520.07, which is a negative resist (Allresist. AR-N 7520.07). It allows performing the large patterns (pads and lines as indicated in Figure 5.2 upper row) by means of optical lithography (L_2), and the smaller features (SiNWs as indicated in Figure 5.2 lower row) by means of electron

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beam lithography (L_3) without an intermediate development step. After the optical and electron beam exposures, the resist is developed, and the remaining resist is used as a mask for pattern transfer in silicon using reactive ion etching. A 100 mm diameter wafer contains more than 6000 SiNW devices

Purpose: The fabrication of silicon nanowire devices requires the simultaneous patterning of high-resolution patterns (nanowires) and large areas (Pads). The process presented allows for a high throughput and high-resolution patterning by using electron and UV optical lithography in the same lithography level. In this way, a whole wafer with thousands of SiNW devices can be patterned in a reasonable amount of time.

Major challenges in process:

- Alignment between EBL and UVL patterns
- Finding compatible conditions for the processing of the mix-and-match resist

Applications:

- Fabrication of nanoelectronics and quantum devices
- High-throughput wafer-scale patterning containing large areas and high-resolution features

Advantages:

- Increased throughput compared with EBL alone
- Increased resolution compared with UV lithography alone
- More affordability compared with DUV or EUV

Limitations:

- Alignment accuracy
- Resist thickness (for pattern transfer)

Process flow:

1. **Wafer cleaning:** Wet etch in successive chemical baths: piranha (H_2SO_4, H_2O_2), HF 5% (10 s), water rinse.
2. **Alignment mark definition** by photolithography with positive-tone HIPR 6512 photoresist.
3. **Pattern transfer** by two Cl-based RIE steps. One to etch the 50 nm top Si layer at 3.3 nm/s, then another at 1.1 nm/s to etch approximately half of the 400 nm buried SiO_2.
4. **Resist removal** by O_2 plasma ashing
5. **Si device definition** by mix-and-match photolithography. The resist layer is 100 nm thick of negative-tone AR-N 7520.07.
6. **Pattern transfer** by Cl-based RIE of the 50 nm top Si layer at 3.3 nm/s.
7. **Resist removal** by O_2 plasma ashing

References:

[1] D. Bricio et al. MNE 2022

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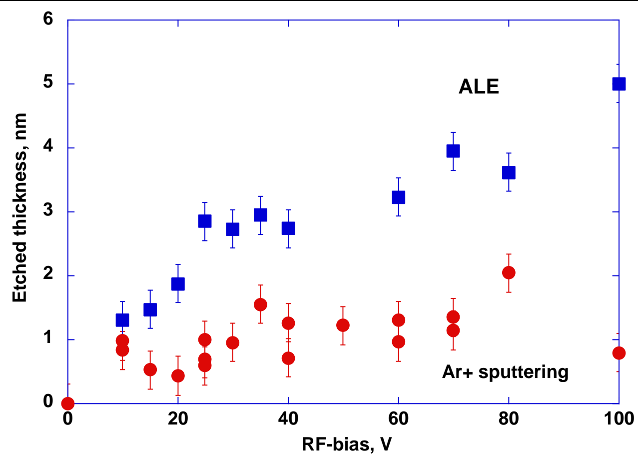
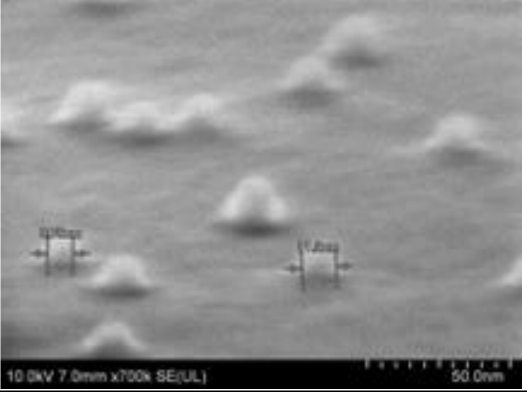
Atomic Layer Etching of Si

Atomic Layer Etching (ALE) of Si using Cl_2/Ar	
	Figure 6.1: Etched Si thickness as a function of Ar+ ion energy (determined by RF-bias) in both ALE (blue dots) and ion sputtering mode (red dots). The number of cycles was kept constant at 25. The activation step was 20 s with a Cl_2 flow of 20 sccm. The etch rate was measured by spectroscopic ellipsometry on silicon-on-insulator (SOI) substrate. The ALE plateau at RF-bias of 25-40 V indicates constant etch per cycle (EPC) typical for the ALE processes.
	Figure 6.2: An example of atomic layer etching of Si using Au aerosol particles as the etch mask. The ALE was performed with 100 cycles in Cl_2/Ar process.

Process: Atomic layer etching is a cyclic process that includes the following steps (a) activation of the etched surface by e.g. adsorption of Cl_2 on Si, (b) purge to remove the excess reactive gas (Cl_2), (c) etching by bombarding the activated (modified) surface by ions with low energy, (d) purge to remove the reaction products. In a perfect ALE process, only a single monolayer is removed (see the plateau in Figure 6.1), however, in practice due to sputtering effects and the presence of reactive gases in the chamber, a thicker layer may be etched in a single cycle. Below are the process conditions that were optimised for implementation of a Si ALE process of Si:

- Tool: ICP-RIE Takachi tool (Plasma Therm, LLC, USA)
- Table below shows the main process conditions of Si ALE. Prior to all etching experiments, native oxide on Si is removed by a short HF-dip. Pieces of SOI about 10x10 mm2 were used for the etching.

ALE STEPS	PROCESS PARAMETERS
Surface activation (dosing)	Cl_2 flow=1-5 sccm Pressure=3 mTorr Time=3-5 s
Dose purge (excess Cl2 removal)	Ar flow=40 sccm Pressure=30 mTorr Time=40 s
Etch step by Ar plasma	RF-power=7-25 W Ar flow=10 sccm Pressure=3 mTorr Time=10 s

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	Etch purge	Ar flow=10 sccm Pressure=30 mTorr Time=2 s	

- Characterisation steps: (a) ellipsometry for SOI samples or (b) SEM cross-section for samples with a mask.

Purpose: The ALE process provides a very accurate control over the removed material, up to a single monolayer (ML) in the best case. Even in a quasi-ALE process where the material removal can exceed the ML, it is possible to etch very precisely.

Major challenges in process:

- Very low etch rate, EPC is about 1 Å per cycle. A quasi-ALE process offers higher etch rate, but it is still well below typical etch rates in RIE. The low etch rate makes it challenging to measure the etched structures.
- Under certain conditions ALE with number of cycles >50 may result in re-deposition of the removed material

Applications: possible applications include etching of Si-based nanostructures, e.g. nanowires or any other structures that require relatively shallow etching (below 40-50 nm).

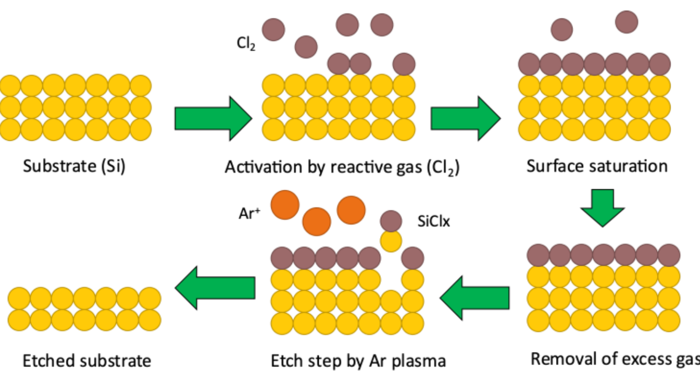
Advantages:

- Extremely good control of the etched material
- Low damage due to a relatively small ion energy

Limitations:

- The EPC is very small, typically 1.3 Å for a "perfect" Si ALE. In practice, a quasi-ALE may be used for etch rates of several Å per cycle.
- The process is currently available for Si only

Process flow:



References:

[1] Park S D, Lee D H and Yeom G Y 2005 Atomic Layer Etching of Si(100) and Si(111) Using Cl[sub 2] and Ar Neutral Beam *Electrochem Solid-state Lett* **8** C106
[2] Oehrlein G S, Metzler D and Li C 2015 Atomic Layer Etching at the Tipping Point: An Overview *Ecs J Solid State Sc* **4** N5041–53
[3] Carver C T, Plombon J J, Romero P E, Suri S, Tronic T A and Turkot R B 2015 Atomic Layer Etching: An Industry Perspective *ECS Journal of Solid State Science and Technology* **4** N5005–9
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[5] Kim D S, Kim J B, Ahn D W, Choe J H, Kim J S, Jung E S and Pyo S G 2023 Atomic Layer Etching Applications in Nano-Semiconductor Device Fabrication *Electron. Mater. Lett.* **19** 424–41
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Talbot Displacement Lithography with Post Processing Steps

Talbot Displacement Lithography (TDL) for sub-80 nm pattern transfer

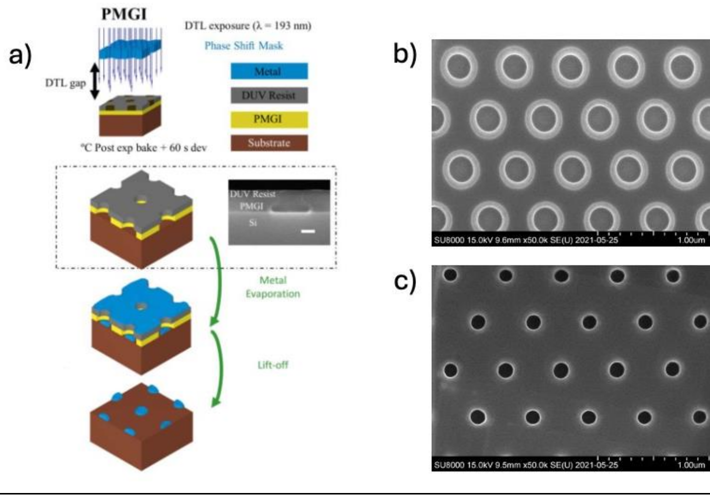

Figure 7.1: a) A schematic process flow of TDL with PMGI layer instead of BARC layer, b) SEM top view of as exposed and developed PAR-PMGI layer with openings of about 240 nm, c) the same sample after the "mix-bake" procedure at 130°C for 120 s. The size of the holes in PAR-PMGI decreased to 150 nm.

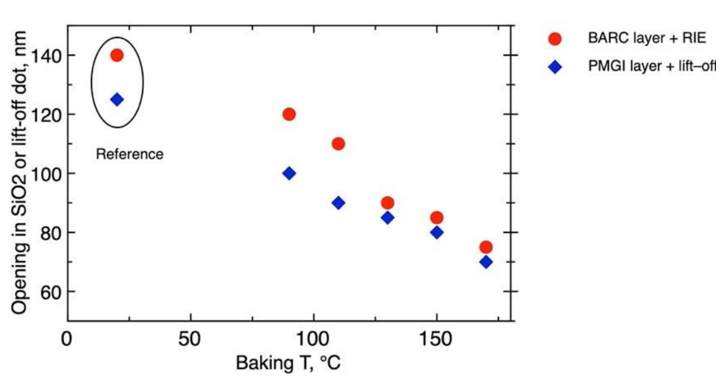

Figure 7.2: Size dependence of Au lift-off circles (blue dots) and etched holes in SiO_2 (red dots) as a function of "mix-bake" post processing temperature. Feature sizes as small as 70 nm on 4" Si wafer have been demonstrated.

Process: The current process of Talbot Displacement Lithography (TDL) [1,2] in combination with a post-processing "mix-bake" step is optimised to form an array of <80 nm holes and lift-off dots on a 4 inch Si wafer. A standard BARC layer has been successfully replaced with PMGI layer to simplify the process flow and improve reproducibility [3]. Further refinement of the process included the use of a AZ-SH114A shrink polymer that is deposited on top of the TDL exposed and developed structure to intermix with the top PAR light-sensitive layer. After annealing, the shrink polymer results in a significant decrease of the size of the openings, see Figure 7.2.

Purpose: one of the main applications of the modified TDL is the fabrication of an array of Au (or other metal) circles for metalorganic vapor phase epitaxy (MOVPE) of III-V nanowires. The method allows very quick processing of the metal arrays on wafers up to 4" in diameter.

Major challenge in process:

- To reproduce the desired size, the exposure dose in TDL should be checked carefully

Applications:

- Formation of arrays of Au seed particles for MOVPE III-V nanowire growth
- Fabrication of large-area nanoimprint stamps using TDL and reactive ion etching (RIE) of SiO_2

Advantages:

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- Very high throughput compared to EBL
- High resolution (about 100 nm after exposure and development) and <80 nm after the "mix-bake" process
- Non-contact method

Limitations:

- Capable of patterning regular structures only
- Every new pattern requires a new mask

Process flow:

PROCESSING STEPS	IMPLEMENTATION
Si substrate with 110 nm thick SiO_2	Thermal oxidation of Si wafer
Deposition of PMGI layer	Spin-coating at 2500 rpm, baking at 200°C, 10 min
Deposition the resist (PAR 1085S90, Sumitomo)	Spin-coating at 2000 rpm, baking at 90°C, 1 min
DTL exposure	Energy 3 J/cm^2, gap distance 80 µm
Resist baking	T=100 °C, 50 s
Resist development	Developer MF24A, 50 s
Deposition of shrink polymer AZ-SH114A	Spin-coating at 1500 rpm, 45 s
Soft baking of the sample	Temperature range: 90-170°C, 120 s
Cooling of the sample	Cool down to room temperature
Development (removal) of AZ-SH114A	Rinsing for 90 s in de-ionised water
Evaporation of Au (or other metal)	Thermal evaporation of a 50 nm thick metal
Lift-off	Lift-off in removal NMP, 2 min
Reactive ion etching of SiO_2 (the alternative to lift-off)	F-based RIE to etch SiO_2. The resist is used as a mask.

References :

[1] Chausse P J P, Boulbar E D L, Lis S D and Shields P A 2019 Understanding resolution limit of displacement Talbot lithography *Opt Express* **27** 5918
[2] Wang L, Clube F, Dais C, Solak H H and Gobrecht J 2016 Sub-wavelength printing in the deep ultra-violet region using Displacement Talbot Lithography *Microelectron Eng* **161** 104–8
[3] Gomez V, Graczyk M, Jam R J, Lehman S and Maximov I 2020 Wafer-scale nanofabrication of sub-100 nm arrays by deep-UV displacement Talbot lithography *Nanotechnology* **31** 1–9

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Silica resist e-beam and He-FIB

Positive-tone resist for electron beam and He-FIB lithography

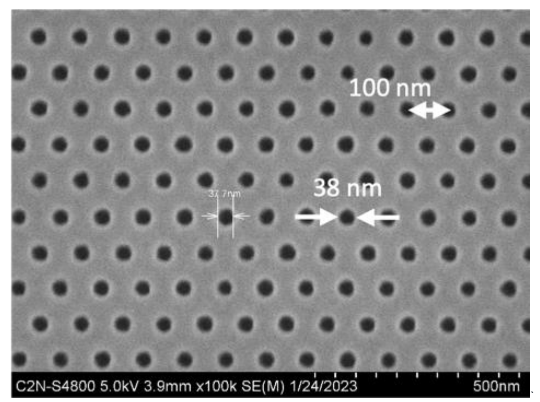

Figure 8.1:
SEM images of 100 nm-thick SiO_2 resist exposed by EBL at 100kV using (dose = 9000 µC/cm²) and developed 15 sec in HF1%.

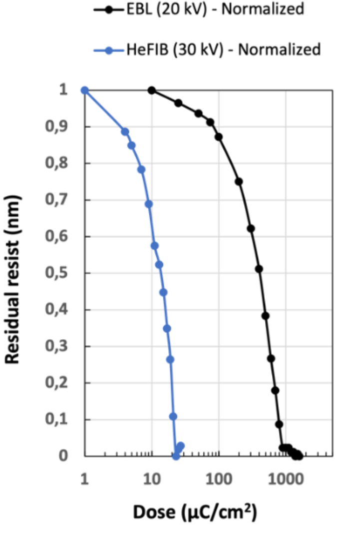

Figure 8.2:
Contrast curves comparison (normalized to the resist thickness) for a SiO_2-based resist (180 nm-thick) exposed at 20 kV by EBL and SiO_2-based resist (215 nm-thick) exposed at 30 kV by He-FIB.

Process: This process describes the synthesis and the development of a new SiO_2-based positive-tone resist for e-beam lithography (EBL) and He-FIB lithography. The resist is based on sol-gel chemistry using Tetraethylorthosilicate (TEOS) and Triethoxymethylsilane (M-TEOS) precursors. The charged beam exposure of the resist promotes the hydrolysis/condensation of an uncondensed (and hydrophobic) hybrid film so that the exposed part and be dissolved in HF1% solution thus resulting in a positive-tone behavior of the resist.

Purpose: Today, the only inorganic resist commercially available for high resolution EBL is the negative-tone Hydrogen Silsesquioxane (HSQ). This new positive-tone inorganic resist complements HSQ with a resolution close to the resolution of PMMA and HSQ.

Major challenges in process: Despite the relatively good resolution and the fact that the synthesis of the resist is straightforward and rapid, the resist still suffers from a relatively short lifetime (few days once stored in fridge), and more investigation is required to understand whether the resist lifetime can be increased to several weeks.
In particular, the hydrolysis/condensation rate of the SiO_2 solution is governed by its PH [1]: this aspect is key to improve the selective dissolution of the exposed/unexposed part (contrast) and the solution lifetime.

Applications: High resolution e-beam and He-FIB lithography for the fabrication of SiO_2 masks. When used as a mask for dry etching of silicon in fluorinated plasmas the selectivity is like HSQ. Higher selectivity and

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resolution can be obtained using alumina resist, a negative-tone resist previously developed in NFFA [1]. Lift-off possible in HF1%.

Advantages:

- Unique positive-tone SiO_2 resist available with such resolution (to our knowledge).
- Possibility to directly pattern SiO_2 masks, for example for the selective growth of nanowires.

Limitations:

- Fast aging (days even in fridge)
- The resist behaves as a positive-tone resist with doses relatively high (yet comparable to HSQ): at 100 kV: 9000-15000 $\mu C/cm^2$ / at 20 kV: 900-1000 $\mu C/cm^2$ / at 30 kV by He-FIB: 11-12 $\mu C/cm^2$. In region overexposed (for example at 20 kV: > 1300 $\mu C/cm^2$) the resist partially recovers a negative-tone character.

References :

[1] Li Voon Ng et al., Macromolecules 28, 6471 (1995)
[2] Cattoni et al., Microelectronic Engineering 193, 18–22 (2018)

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Selective area growth of III-V nanowire

Positive-tone resist for electron beam and He-FIB lithography

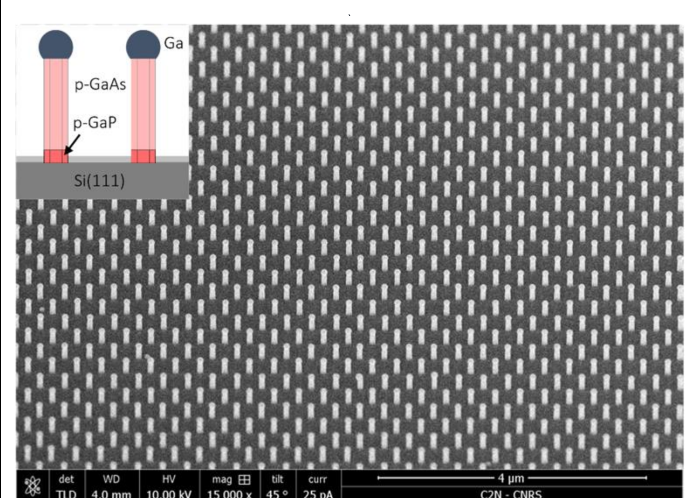

Figure 9.1:
SEM images of an hexagonal array (pitch 360 nm) of self-catalyzed GaP/GaAs nanowires grown on Si(111) by MBE using the Vapor-Liquid-Solid method (VLS).

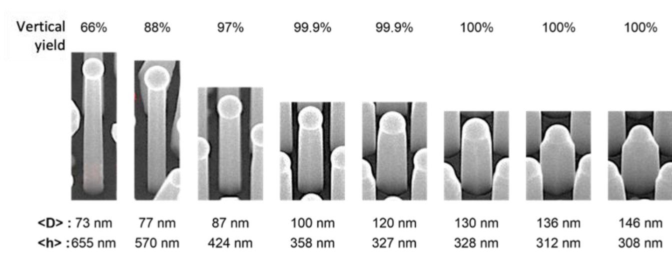

Figure 9.2:
SEM images of representative self-catalyzed GaP/GaAs nanowires grown on Si(111) using the Vapor-Liquid-Solid method (VLS) in the same MBE growth and a SiO_2 mask with different average diameters <D>, average height <h> (measured on 10 different NWs per group). The corresponding yield of vertical NWs is indicated.

Process: This process describe the preparation of the Si(111) substrate and the epitaxial growth of self-catalyzed III-V semiconductor nanowires by MBE using the Vapor-Liquid-Solid method (VLS) to achieve yield of vertical nanowires close to 100% over the whole surface area (demonstrated up to 2 inches).

Purpose: The selective area growth of III-V NW is typically obtained by pattering a thin SiO_2 (or SiN) mask on Si(111) substrate by electron beam and dry etching; the selective growth is performed by Vapor-Liquid-Solid (VLS) method using a Gallium catalyst (self-catalyzed growth) by MBE or MOVPE. The two main problems using this method are the difficulty in obtaining reproducibly high yield of vertical NWs [1] [2] and the difficulty to tune the NWs diameters, which tend – independently from the nanohole opening diameter and the Ga-droplet dimensions – to converge to fixed diameter (80-90 nm). The proposed technology solves these two issues obtaining high (>99%) yield of vertical NWs and the control of the NWs diameters from the beginning of the growth (that is, using only VLS growth without any contribution from the Vapor Solid growth).

Major challenges in process:

- CCP-RIE time must be calibrated carefully (Process flow step n° 4).
- To achieve a specific NW diameter without tapering, the growth conditions (Ga pre-deposition and V/III ratio), must be chosen carefully in accordance to the desired NW diameter and the pitch of the array
- For relatively long NWs (>> array pitch) shadowing effects [3] may require changing the V/III ratio during growth to avoid tapering.

Applications: selective area growth of III-V NW on Si(111), demonstrated for $Ga_{1-x}AsP_x$ (x=0÷1), but in principle adaptable to the growth of other III-V or II-VI semiconductor NWs.

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Advantages:

- Allows reproducible and robust high yield of vertical NWs over large surface areas (thanks to modified-Marangoni drying)
- Allows the control of the NWs diameters from the beginning of the growth (using only VLS growth without any contribution from the Vapor Solid growth).

Limitations:

- Higher yields are achieved using GaP foot (lattice-matched to Si), while direct growth of GaAs give rises to slightly lower yield of vertical NWs. More investigation is needed on this particular case.

Process flow:

1. **Si(111) surface preparation:** 3 cycles of oxidation-etching are performed to ensure an ultra-clean silicon wafer surface using a CCP-RIE oxygen plasma (high bias) + HF5%.
2. **SiO_2 mask deposition:** Plasma-enhanced chemical vapor deposition (PECVD) of thin layer of SiO_2 (50-70 nm).
3. **Lithography:** electron-beam lithography (EBL) using positive-tone resist (495PMMA, 2%) of a hexagonal hole pattern using a Vistec EBPG 5000+/5200 system operating at 100 kV.
4. **Pattern transfer in SiO_2 mask:** the hexagonal hole pattern in the PMMA is transferred to the SiO_2 mask by CCP-RIE using a mixture of SF_6 and CHF_3 gases. Etching time requires fine calibration to prevent the damage of the Si(111) surface.
5. **Holes "development":** removal of the thin SiO_2 layer left inside the nanoholes after CCP-RIE using HF 1% solution for 30 sec, rinsing in DI and N_2 drying.
6. **Modified-Marangoni drying:** high yields of vertical NWs over large areas (2 inches) can only be obtained by drying the sample using a modified-Marangoni drying using a mixture of N_2/2-methoxyethanol while keeping the substrate at 105°C during the withdrawal from the DI (the fundamental difference between the Marangoni drying [4] on Si and our modified-Marangoni drying on SiO_2 surface stems from the fact that the former works on Si (hydrophobic) at RT, the latter is adapted to SiO_2 (hydrophilic) at $T > T^{H2O\ boiling\ temperature}$.
7. **Epitaxial growth:** sample loaded in the MBE; 20 min thermal annealing at 750°C; Ga pre-deposition typically with a Ga flux corresponding to a two-dimensional GaAs equivalent growth rate of 0.71 ML/s (2 Å/s); growth of a short GaP segment followed by GaAs growth (resulting in a linearly graded GaP/GaAs transition); GaAs NWs are then grown under an As_4/Ga flux ratio of about 1.2. The ratio should be changed and optimized depending on the desired NW diameter and tapering.

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